Application Number 10/824942
Response to Office Action dated 03/30/2007 and
Response to Notice of Non-Compliant RCE dated 08/13/2007

REMARKS

Applicant submits this amendment as a submission required by 37 CFR 1.114 in response to the Notice of Improper Request for Continued Examination mailed 13 August 2007. Applicants amend claims 1 and 5. In amending claims 1 and 5, Applicants have not added new matter; support for the dummy diffused region being capable of supplying a collector current of a parasitic transistor is given on page 6, lines 11-12. Claims 2-4 and 6 were canceled previously. Claims 1 and 5 are pending.

The Rejection under 35 U.S.C. §102(b) by Ishikura '556

Applicant traverses the rejection of claim 1 as being anticipated by Ishikura '556. Claim 2, also rejected, is canceled. Applicant does not concede the correctness of the rejection of the claims. Applicant's traversal of the rejection is based in part because Ishikura '556 does not teach or suggest that the collector current of the parasitic transistor is supplied from the dummy diffused region, as required by claims 1 and 5.

Nor can the limitation that the collector current of the parasitic transistor be supplied from the dummy diffused region be obvious, given the teachings of Ishikura '556. As shown in Applicant's Figure 4, a dummy diffused region is located between an area under the dummy layer part and either the digital circuit part or the analog circuit part. As shown in Figure 5B of Ishibura '556 and according the rejection, however, a dummy diffused region 11a is located under a dummy layer 13a between the digital and analog circuit parts, and is not under either the digital or the analog circuit part. Additionally, Ishibura '556 does not teach a power-supply voltage applied to the dummy diffused region. Because of these shortcomings, i.e., because there is no voltage applied to the dummy diffused region and because the dummy diffused region of is not located under either the analog circuit part or the digital circuit part, the dummy diffused region cannot provide the collector current as claimed.

Applicant requests that the rejection of claim 1 be withdrawn in view of the amendment and the remarks above.

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The Rejection under 35 U.S.C. §103(a)

Applicants traverse the rejection of claim 5 as being obvious over the prior art admitted by Hasegawa '927 in view of Ishikura '556. Applicant canceled claim 3 so the rejection is moot. Applicant, however, does not concede the correctness of the rejection. With respect to claim 5, neither the prior art admitted by Hasegawa '927 nor Ishikura '556 teach or suggest a camera having a semiconductor integrated circuit device in which the semiconductor integrated circuit device has a dummy diffused region located under a dummy layer part and either the digital circuit part or the analog circuit part. The rejection admits that Hasegawa '927 does not teach a dummy polysilicon region between the digital and analog circuits, but Claim 5 requires that the dummy diffused region be provided between the dummy layer part and either the digital circuit part or the analog circuit part, i.e., the dummy diffused region is under at least one circuit part and is not between the circuit parts. Again, this allows the dummy diffused region to act as a parasitic transistor supply a collector current so that the voltage of the well region is stabilized, which in turn provides a more reliable image sensor device.

Because neither Hasegawa '927 nor Ishikura '556 teach or suggest a camera having a semiconductor integrated circuit that has a dummy region that creates a parasitic transistor to supply a current to stabilize the performance of the circuit or the camera having the semiconductor integrated circuit, Applicant asserts that claim 5 is allowable.

If any further issues remain that can easily be resolved by telephone, the Examiner is requested to telephone the Attorney below, Douglas P. Mueller at 612.455.3804.

Respectfully submitted,

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Dated: August 30, 2007

By: _____
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